ABSTRACT

A method and system for providing a power enhanced lateral DMOS device is disclosed. The method and system comprise providing a semiconductor substrate with a plurality of source/body structures thereon. The method and system further comprise providing a slot in the semiconductor substrate between the plurality of source/body structures to provide a truncated source; and providing a metal within the slot to provide a ground strap device. The method and system in accordance with the present invention offers the following advantages:

1. Increases the snap back (sustaining) voltage when integrated with the EDLDMOS to the point where the device is limited by breakdown voltage of the drain/body – which is a much higher voltage than the normal snap back (sustaining) voltage.

2. Improves the gm of the device for several reasons, one of which is the fact that the device can be operated at higher current (optimum for the design where the gm peaks prior to being limited by snap back voltage) and voltage prior to being limited.

3. Reduces the capacitance of the device – drain to body capacitance is reduced due to the smaller area.

4. Reduces Ron due to the short and robust ground strap providing a lower source resistance than other approaches. The drain metal is supplied in a slot which reduces any loss due to drain resistance.

5. Increases the frequency of operation due to higher gm and lower capacitance.

6. Increases the protection against electromigration due to the heavier ground buss and improved heat transfer.

7. Reduces noise that is normally generated at the source/body as it approaches snap

back and due to feedback from other circuits or the power supply. Reduces noise also in the power supply lead since it is a lower resistance buss due to the thick metal buried power buss.

8. Reduces the die size since there is space required for an interconnect to ground and there is no isolation diffusion which takes up considerable room. The device is isolated by the ground strap throughout the device design. The power lead is oxide surrounded and therefore can be moved closer to active or passive elements within the die.

9. Increase the net die per wafer due to the smaller die size resulting in more gross die per wafer and reduced loss due to defect density issues due to the reduction in die size. Improves the yield since yield is a function of die size.

10. Improves the heat transfer due to the intimate contact with the silicon. Heat transfer through silicon is 10 times better than through an oxide and 200 times better than through air.

11. Provides an IU versus a junction isolated structure and the frequency response advantages of this very significant feature. This also results in die size reduction since the oxide isolated grounds throughout the structure take up much less room than the normal isolation diffusion type structure.

12. Allows the standard process to remain intact till near the end of the standard process prior to implementation.